WHAT IS CLAIMED IS:

- 1. A capacitor device, comprising:
- a first electrode located over a substrate and connected to a first interconnect;
- a first insulating layer located over the first electrode;
- a second electrode located over the first insulating layer and connected to a second interconnect;
 - a second insulating layer located over the second electrode; and
- a third electrode located over the second insulating layer and connected to the first interconnect.
- 2. The capacitor device recited in Claim 1 wherein the third electrode is located over the first and second electrodes.
- 3. The capacitor device recited in Claim 1 further comprising a third insulating layer located over the third electrode, wherein the first and second interconnects are located over the third insulating layer.
 - 4. The capacitor device recited in Claim 1 wherein:
 the first electrode and the first interconnect are connected by a first via;
 the second electrode and the second interconnect are connected by a second via; and
 the third electrode and the first interconnect are connected by a third via.

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5. The capacitor device recited in Claim 4 wherein at least one of the first, second and third vias and at least one of the first and second interconnects are collectively a dual-damascene structure.

6. The capacitor device recited in Claim 1 wherein the first insulating layer includes an insulation layer and an etch stop layer located over the insulation layer.

7. The capacitor device recited in Claim 1 wherein a first perimeter of the first electrode envelopes a second perimeter of the second electrode.

8. The capacitor device recited in Claim 7 wherein the second perimeter envelopes a third perimeter of the third electrode.

9. The capacitor device recited in Claim 1 wherein the first electrode comprises copper.

10. The capacitor device recited in Claim 1 wherein the second and third electrodes each comprise a same one selected from the group consisting of:

tungsten;

tungsten silicide;

aluminum;

titanium; and

titanium nitride.

- 11. The capacitor device recited in Claim 1 wherein the second and third electrodes each include a plurality of conductive layers.
- 12. The capacitor device recited in Claim 1 wherein a total unit capacitance of the capacitor device ranges between about 1.3 fF/μm² and about 2.0 fF/μm².
- 13. The capacitor device recited in Claim 1 wherein a total unit capacitance of the capacitor device is about 1.5 fF/ μ m².
- 14. A method of manufacturing a capacitor device, comprising:

 forming a first interconnect over and coupled to a first electrode;

 coupling the first interconnect to a second electrode formed over the first electrode; and

 forming a second interconnect over and coupled to a third electrode, the third electrode

 interposing the first and second electrodes.
- 15. The method recited in Claim 14 further comprising:

 forming a first insulating layer interposing the first and third electrodes;

 forming a second insulating layer interposing the second and third electrodes; and

 forming a third insulating layer interposing the second electrode and the first and second
 interconnects.

- 16. The method recited in Claim 15 wherein the first interconnect is a dual-damascene structure having:
 - a trench portion over the third insulating layer, and
 - a via portion extending through at least the first and third insulating layers.
- 17. The method recited in Claim 15 wherein forming the first insulating layer includes forming an insulation layer and forming an etch stop layer over the insulation layer.
- 18. The method recited in Claim 14 wherein at least one of the first, second and third electrodes comprises a plurality of conductive layers.
 - 19. A semiconductor device, comprising:
 - a transistor element located over a substrate and having a contact;
 - a capacitor element, including:
 - a first electrode located over the substrate;
 - a first insulating layer located over the first electrode;
 - a second electrode located over the first insulating layer;
 - a second insulating layer located over the second electrode; and
 - a third electrode located over the second insulating layer;
 - a dielectric layer located over the transistor element and the capacitor element;
- a first interconnect located over the dielectric layer, coupled to the first electrode by a first via, and coupled to the third electrode by a second via; and

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a second interconnect located over the dielectric layer, coupled to the second electrode by a third via, and coupled to the transistor contact by a fourth via.

- 20. The semiconductor device recited in Claim 19 wherein the first interconnect and the first and second vias are collectively a dual-damascene structure.
- 21. The semiconductor device recited in Claim 19 wherein the second interconnect and the third and fourth vias are collectively a dual-damascene structure.
- 22. The semiconductor device recited in Claim 19 wherein the first insulating layer includes an insulation layer and an etch stop layer located over the insulation layer.
- 23. The semiconductor device recited in Claim 19 wherein the first electrode comprises copper.
- 24. The semiconductor device recited in Claim 19 wherein the second and third electrodes each comprise a same one selected from the group consisting of:

tungsten;

tungsten silicide;

aluminum;

titanium; and

titanium nitride.

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25. The semiconductor device recited in Claim 19 wherein the second and third electrodes each include a phrality of conductive layers.